REMARKS

The Examiner has reminded the Applicants of the proper content of the abstract. However, the Examiner has not objected to the abstract or portion thereof and has not requested the Applicants to amend the abstract.

The Examiner objected to claims 11, 17 and 27, stating "Claims 11, 17 and 27 are objected to because of the following informalities: a) Please change "supply power" to "supplying power" in lines 2 and 8 of claim 11. b) Please change "said power" to "said first power" in line 6 of claim 17. c) Please change "supply power" to "supplying power" in lines 2 and 5 of claim 27. Appropriate correction is required.." In response, Applicants have amended claims 11, 17 and 27 as the Examiner has requested.

The Examiner rejected claims 1-32 under 35 U.S.C. 103(a) as being unpatentable over Radjassamy (Us. PN: 6,331,800) in view of Tsinker (U.S. PN: 6,323,692).

Applicants respectfully traverse the §103(a) rejections with the following arguments:

35 USC § 103 Rejections

As to claims 1 and 7, the Examiner states that "Radjassamy in figure 3 disclose or teach an integrated circuit comprising a first latch (302) coupled to first clock signal (CK1N) and first logic (304), second latch (306) coupled to second clock signal (CK2N) and second logic (308) for adjusting of clock edge rise/fall times between non-overlapping clock signals and thereby eliminate a race (see col. 1, lines 5-9). Further, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal

which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Although, Radjassamy **do not explicitly** show or teach power (rails) applied to the latches and logic circuits, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuits (see abstract) and further Radjassamy in figure 2 disclose a voltage supply (VDD) applied to a clock and a logic block. **However,** Tsinker in figure 1 disclose a compensation circuit (10) comprise a clock generator or a square wave generator (14) wherein the square wave generator is a rail-to-rail signal having a voltage amplitude referenced to ground or other voltage potential, as used herein, the term rail-to-rail square wave signal means, when low, is set to voltage supplied by a first power rail (e.g., ground) and when, high is set to a voltage supplied by a second power rail (e.g., VDD) (see col.7, lines 50-60). Further Tsinker teach that the compensation circuit comprise a phase comparator whereby the phase comparator have first and second latches for receiving and outputting control signals wherein the control signals having first and second logical states (see col. 4, lines 8-68 and col. 5, lines 1-12). **Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to implement the teachings of Radjassamy to include power supplies for powering clocks and latches as taught by Tsinker. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to vary certain limits, for example; longer time at higher voltage, allows reduced temperature or higher voltage at higher temperature, allows reduced time."

First, Applicants cannot find any teaching, suggestion or incentive for modifying Radjassamy with Tsinker in either Radjassamy or Tsinker. Absent such showing in the prior art, Applicants contend that the Examiner has impermissibly used the Applicants' teaching to hunt

through the prior art for the claimed elements and combine them as claimed in violation of *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed Cir. 1991); *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed Cir. 1990) and *In re Laskowski*, 871, 910 F.2d 115, 117, 10 USPQ2d 1397, 1398 (Fed. Cir. 1989) and request that the rejection of claims 1 and 6 be withdrawn.

Second, the motivation cited by the Examiner, namely "**This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to vary certain limits, for example; longer time at higher voltage, allows reduced temperature or higher voltage at higher temperature, allows reduced time" is incompatible with the operation of Applicants invention. Applicants' invention would **decrease not increase** the time spent at higher voltage and would **increase not decrease** stress time since in Applicants' invention voltage is applied to each set of latches and circuits only during one phase of the clock.

Third, Applicants contend that claims 1 and 6, as amended, are not obvious in view of Radjassamy in view of Tsinker because Radjassamy in view of Tsinker does not teach or suggest every feature of claims 1 and 6.

As a first example, Radjassamy in view of Tsinker does not teach or suggest in the case of claim 1,"a first power rail for supplying power to first latch and a circuit only during a first clock phase, said first power rail supplied from a first power supply" or in the case of claim 6, "a first power rail for supplying power to an L1 latch of an L1/L2 latch only during a first clock phase, said first power rail supplied from a first power supply." As a second example, Radjassamy in view of Tsinker does not teach or suggest in the case of claim 1 " said second power rail supplied from a second power supply" or in the case of claim 6 "a second power rail for supplying power to an L2 latch of said L1/L2 latch and to a circuit coupled to an output of

said L2 latch only during a second clock phase, said second power rail supplied from a second power supply."

Applicants respectfully point out that the first and second power rails of Tsinker are rails of the same power supply as stated in col. 7, lines 53 to 58, to wit "As used herein, the term rail-to-rail square wave signal means a square wave that, when low, is set to a voltage supplied by a first power rail (e.g. ground) and, when high, is set to a voltage supplied by a second power rail (e.g. VDD or about 3 to 3.6 volts)." Applicants further point out that neither Radjassamy or Tsinker teach or suggest coupling some power rails to some latches and circuits and other power rails to other latches and circuits. Further Applicants respectfully point out that neither Radjassamy or Tsinker teach or suggest what combination of power rails to couple to which latch or which circuit.

Based on the preceding arguments, Applicants respectfully maintain that claims 1 and 6 are not unpatentable over Radjassamy in view of Tsinker and are in condition for allowance. Since claims 2-5 depend from claim 1, and claims 7-10 depend from claim 6, Applicants respectfully maintain that claims 2-5 and 7-10 are likewise in condition for allowance.

As to claims 2 and 7, the Examiner states "Radjassamy in view of Tsinker teach all the subject matter claimed in claims 1 and 6 including Radjassamy in figure 3 disclosed second latch (308) coupled to the second logic (circuit) (306) whereby the second latch and the second logic circuit coupled to the second clock (CK2N)."

Applicants contend that claims 2 and 7 are not obvious in view of Radjassamy in view of Tsinker because Radjassamy in view of Tsinker does not teach or suggest every feature of claim 2 and 7. For example in the case of claim 2, Radjassamy in view of Tsinker does not teach or suggest "a second circuit coupled to an output of said second latch and powered from said

second rail." For example in the case of claim 7, Radjassamy in view of Tsinker does not teach or suggest "said L1 latch of said second L1/L2 latch powered by said first power rail and an L2 latch of said second L1/L2 latch powered by said second power rail." Applicants respectfully point out that neither Radjassamy or Tsinker teach or suggest what combination of power rails to couple to which latch or which circuit. Based on the preceding arguments, Applicants respectfully maintain that claims 2 and 7 are not unpatentable over Radjassamy in view of Tsinker and are in condition for allowance

As to claims 3-5 and 8-10, the Examiner states that " Radjassamy in view of Tsinker teach all the subject matter claimed in claims 1 and 6 including Tsinker in figure 1 disclose a compensation circuit (10) comprise a clock generator or a square wave generator (14) wherein the square wave generator is a rail-to-rail signal having a voltage amplitude referenced to ground or other voltage potential, as used herein, the term rail-to-rail square wave signal means, when low, is set to voltage supplied by a first power rail (e.g., ground) and when, high is set to a voltage supplied by a second power rail (e.g., VDD) (see col. 7, lines 50-60)."

Applicants contend that claims 3 and 8, as amended, are not obvious in view of Radjassamy in view of Tsinker because Radjassamy in view of Tsinker does not teach or suggest every feature of claims 3 and 8. For example, Radjassamy in view of Tsinker does not teach or suggest "said first and second clocks powered from a third power rail." Applicants respectfully point out that only two rails (albeit from the same power supply) are taught by Tsinker. Based on the preceding argument, Applicants respectfully maintain that claims 3 and 8 are not unpatentable over Radjassamy in view of Tsinker and are in condition for allowance.

Claims 4 and 9 teach an overlapping relationship between the state of each clock phase only during de-powering and powering. Radjassamy specifically teaches non-overlapping clock

signals (see Radjassamy col. 1 lines 5-9), thus teaching away from Applicants' invention. Based on the preceding arguments, Applicants respectfully maintain that claims 4 and 9 are not unpatentable over Radjassamy in view of Tsinker and are in condition for allowance.

As to claims 11-16, the Examiner states "Radjassamy substantially teach or disclose an integrated circuit comprising clocked logic gates a method for increasing the rise/fall of clock edges in an IC commencing with the identification (detecting) of a clock signal with a clock edge having a poor rise/fall time (see abstract and col. 3, lines 34-43). Further, Radjassamy in figure 3, disclose first latch (302) coupled to first clock signal (CK1N) and first logic (304), second latch (306) coupled to second clock signal (CK2N) and second logic (308). Furthermore, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Although, Radjassamy **do not explicitly** show or teach power (rails) applied to the latches and logic circuits, Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuits (see abstract) and further Radjassamy in figure 2 disclose a voltage supply (VDD) applied to a clock and a logic block. **However,** Tsinker teach that a circuit comprise a phase comparator having a phase comparator including first and second latches for receiving and outputting control signals wherein the control signals having first and second logical states (see col. 4, lines 8-68 and col. 5, lines 1-12) and further Tsinker teaches a method for setting voltages supplied by power rails (as ground and VDD) inputted to clocks and latches (see col. 7, lines 5060). **Therefore,** it would have been obvious to a person having an ordinary

skill in the art at the time the invention was made to implement the teachings of Radjassamy to include power supplies for powering clocks and latches as taught by Tsinker. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated in order to vary certain limits, for example; longer time at higher voltage, allows reduced temperature or higher voltage at higher temperature, allows reduced time."

Applicants note that claims 11-16 include all the elements of claims 1- 5 and additionally add limitations related to third and fourth power rails and that the Examiners stated reasons for rejecting claims 11-16 are essentially identical to those given for rejecting claims 1-5. Therefore Applicants contend all of Applicants' arguments *supra* in respect to claims 1-5 are applicable to claims 11-16. Based on the preceding arguments, Applicants respectfully maintain that claims 11-16 are not unpatentable over Radjassamy in view of Tsinker and are in condition for allowance.

As to claims 17 and 22, the Examiner states "Radjassamy in view of Tsinker teach or disclose all the subject matter claimed in claims 1 and 6, including Radjassamy teach a method of increasing the rise/fall time of clock edges in an integrated circuit, thereby providing a means for eliminating races, a means for otherwise adjusting non-overlapping clock signal dead times, or a means for adjusting clock pulse widths and the method commences with the identification of a clock signal which has a clock edge with a poor (or inadequate) rise/fall time and when a circuit is simulated the clock edges transmitted in a square wave fashion (see col. 4, lines 1-14). Radjassamy in view of Tsinker **do not explicitly** teach or mention the testing as a stress testing, However, Radjassamy teach a method for eliminating races commences with testing of IC for races (see abstract) and a method of increasing the rise/fall time of clock edges (see abstract) which is basically used a method for stressing the IC device. **Therefore,** it would have been

obvious to a person having an ordinary skill in the art at the time the invention was made to stress an IC device by powering the IC and observe the result. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the using power raids by powering / de-powering for stressing an IC are well known futures and functionalities of integrated circuits."

Applicants believe that the Examiner has repeated a portion of the arguments used by the Examiner in rejecting claims 1 and 6 but has changed the motivation for modifying the references. Applicants contend that Applicants' arguments given *supra* in respect to claims 1 and 6 are applicable to claims 17 and 22. The Examiners states as new motivation for modifying Radjassamy with Tsinker, that "**Therefore,** it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to stress an IC device by powering the IC and observe the result. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the using power raids by powering / de-powering for stressing an IC are well known futures and functionalities of integrated circuits." Applicants contend that the new motivation suggested by the Examiner is not found in either Radjassamy or Tsinker and thus constitutes a violation of *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed Cir. 1991); *In re Bond*, 910 F.2d 831, 15 USPQ2d 1566 (Fed Cir. 1990) and *In re Laskowski*, 871, 910 F.2d 115, 117, 10 USPQ2d 1397, 1398 (Fed. Cir. 1989) and request that the rejection of claims 17 and 22 be withdrawn. Further, the Examiners has failed to connect the stated motivation with any element of claims 17 or 22 and has thus an improperly shifted of the burden of establishing *prima facie* obviousness from the Examiner to the Applicant. Based on the preceding arguments, Applicants respectfully maintain that claims 17 and 22 are not unpatentable over Radjassamy in view of Tsinker and are in condition for

allowance. Since claims 18-21 depend from claim 17 and claims 23-26 depend from claim 22, Applicants respectfully maintain that claims 18-21 and 23-26 are likewise in condition for allowance.

As to claims 18-20 and 23-25, Applicants maintain that the Examiners arguments are the same as those given for rejecting claims 2-4 and 7-9 and Applicants' arguments *supra* with respect to claims 2-4 and 7-9 are applicable to claims 18-20 and 23-25. Based on the preceding arguments, Applicants respectfully maintain that claims 18-20 and 23-25 are not unpatentable over Radjassamy in view of Tsinker and are in condition for allowance

As to claims 27-32 the Examiner states that "Radjassamy in view of Tsinker teach all the subject matter claimed in claim 11. Radjassamy in view of Tsinker **do not explicitly** teach or mention the testing as a stress testing, However, Radjassamy teach a method for eliminating races commences with testing of IC for races (see abstract) and a method of increasing the rise/fall time of clock edges (see abstract) which is basically used a method for stressing the IC device. **Therefore**, it would have been obvious to a person having an ordinary skill in the art at the time the invention was made to stress an IC device by powering the IC and observe the result. **This modification** would have been obvious because a person having ordinary skill in the art would have been motivated to do so because the using power raids by powering / de-powering for stressing an IC are well known futures and functionalities of integrated circuits."

Applicants believe that the Examiner has repeated a portion of the arguments used by the Examiner in rejecting claim 11 but has changed the motivation for modifying the references to that used for rejecting claims 17 and 22. Applicants contend that Applicants' arguments given *supra* in respect to claims 17-20 and 22-25 are applicable to claims 31 as are Applicants arguments *supra* in respect to claims 11-16.

Based on the preceding arguments, Applicants respectfully maintain that claims 27-32 are not unpatentable over Radjassamy in view of Tsinker and are in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that claims 1-32 meet the acceptance criteria for allowance and therefore request favorable action. If Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invite the Examiner to contact the Applicants' representative at the telephone number listed below.

Respectfully submitted,

Dated: 03/24/2004

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